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Semiconductor device having intermediate layer for pinching off conductive path during reverse bias application.

A semiconductor device comprising a semiconductor substrate (30) having two major surfaces, cathode electrode film (32) formed on the first major surface of the substrate (30), and anode electrode film (34) made of a Schottky-barrier metal such as titanium (Ti, Mo, V), formed on the second major surface of the substrate (30). The substrate (30) is formed of an N⁺-type layer (36) formed on the cathode electrode film (32), an N⁻-type layer (38) formed on the N⁺-type layer (36), an N⁻-type layer (40) formed on the N⁻-type layer (38) and having an impurity concentration lower than that of the N⁻-type layer (38), and an N⁻-type layer (42) interposed between the N⁻-type layer (40) and the anode electrode film (34). The device further comprises a plurality of P⁺-type areas (46) formed in the second major surface of the substrate (30), contacting the anode electrode film (34) and extending through the N⁻-type layer (42) and the N⁻-type layer (40) into the N⁻-type layer (38). When a forward bias is applied to the device, a current flows from the anode electrode film (34), passes through the N⁻, N⁻, N⁻ and the N⁺-type layers (42, 40, 38, 36), and flows out of the cathode electrode film (32). When a reverse bias is applied to the device, the depletion layer formed around the junction between each P⁺-type area (46) and the N⁻-type layer (40) extends, joining with the similar depletion layers, thereby pinching off the path of the current. As a result, the flow of a reverse leakage current is suppressed.

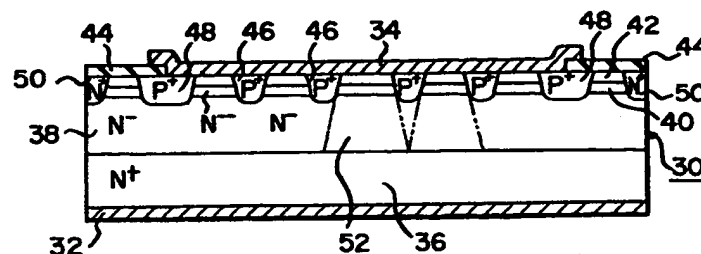


FIG. 5

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EP 0 372 428 A1

Semiconductor device having intermediate layer for pinching off conductive path during reverse bias application

The present invention relates to a semiconductor device comprising a Schottky barrier diode wherein a PN junction is formed on a semiconductor layer located below a barrier metal film, and more particularly, to a semiconductor device having an intermediate semiconductor layer for pinching off a conductive path during the application of a reverse bias.

5 Recently, most components of electronic apparatuses are ICs, and the power-supply devices incorporated in these apparatuses are generally switching regulator which are small and light and also operate with high efficiency. Most of the switching regulators have a Schottky Barrier Diode SBD rectifier used as output rectifying element. The SBD rectifier has a small forward voltage drop V_F and a short reverse-recovery time. However, the JBS rectifier now widely used is disadvantageous in two respects. First, a
10 relatively large reverse leakage current flows in it. Second, its reverse breakdown voltage is low.

A new type of a SBD rectifier has been developed in which a small reverse leakage current flows, and whose reverse breakdown voltage is sufficiently high. (See Published Examined Japanese Patent Application No. 59-35183.) Such a rectifier is called Junction Barriers Schottky (JBS). As is shown in Fig. 1, the substrate 10 of this JBS rectifier comprises an N^+ -type silicon layer 12, an N^- -type silicon layer 14 formed
15 on the layer 12 by means of epitaxial growth. Metal electrode film 16 is formed on the lower surface of the layer 12. A plurality of P^+ -type silicon areas 18 are formed in the upper surface of the layer 14. Oxide film 20 having an opening is formed on the upper surface of the layer 14. Metal film 22, for example, chromium film, which forms a Schottky barrier, is formed partly on the exposed portion of the layer 14 and partly on the oxide film 20, as is illustrated in Fig. 1. The areas 18 are spaced apart from one another, for such a
20 distance that depletion layer which they are connected by a extending depletion layer 24 when a negative voltage are applied to the layer 16 and the film 22, respectively.

When a forward voltage is applied to the JBS rectifier shown in Fig. 1, most of a forward current flows through the Schottky barrier formed of the metal film 22 and the N^- -type silicon layer 14, as is shown by arrows A. Hence, the forward voltage drop in this JBS rectifier is nearly equal to that in the ordinary
25 Schottky diode which has no P^+ -type silicon areas.

A depletion layer 24 is formed in the PN junction comprised of the N^- -type silicon layer 14 and the P^+ -type silicon area 18. As the reverse bias is increased, the their depletion layer 24 connects one another. The joint depletion layer 24' causes to control the reverse leakage current to decrease. As a result, the reverse-current characteristic of the JBS rectifier becomes similar to that of a PN junction diode, and the
30 breakdown voltage of the JBS rectifier is improved.

If the reverse bias applied to the JBS rectifier is too low, depletion layers 24 cannot be connected to each other. Hence, the reverse leakage current, which flows through the Schottky barrier formed of the N^- -type silicon layer 14 and the metal film 22, is not much influenced. The reverse-current characteristic of the JBS rectifier cannot be greatly improved until the reverse bias increases so much that the depletion layer
35 24 connects one another.

Fig. 2 is a sectional view showing the JBS rectifier disclosed in Published Unexamined Japanese Patent Application No. 60-74582 and also in by B.J. Baliga, IEEE, Electron Device Letter, Vol. DEL-5, No. 6, 1984, pp. 194-196. As is shown in Fig. 2, wherein the same reference numerals are used, denoting the elements identical or similar to those illustrated in Fig. 1, a plurality of PN junctions is formed in the surface of that
40 portion of a semiconductor substrate 10 on which barrier metal film 22 is formed.

The semiconductor substrate 10 is made of an N^+ -type silicon layer 12 and an N^- -type silicon layer 14. The barrier metal film 22 is made of aluminum. Generally, it is necessary to form a thin N^+ -type silicon layer in the surface of N^- -type silicon layer 14 by means of ion implantation, thereby to reduce the height of the Schottky barrier formed of N^- -type silicon layer 14 and the metal film 22. In the JBS rectifier shown in
45 Fig. 2, such a thin N^+ -type silicon layer is not formed since the film 22 is made of metal (ex. Ti, Mo, V) which has a low Schottky-barrier property. A plurality of P^+ -type silicon areas 18 are formed in the upper surface of a portion of the N^- -type silicon layer 14. A guard ring 26 is formed on the layer 14, surrounding that portion of the layer 14. The guard ring 26 imparts an adequate breakdown voltage to the JBS rectifier.

When a forward bias is applied to the JBS rectifier, depletion layers 24 are formed, each being an PN junction between a P^+ -type silicon areas 18 and the N^- -type silicon layer 14. The depletion layers 24 are not connected to one another when a forward bias is applied to the JBS rectifier. In other words, the depletion layers 24 are spaced apart by a gap 28 as is indicated by broken lines in Fig. 2, thereby allow the passage of a forward current. When a reverse bias is applied to the JBS rectifier, a single depletion layer 24' is formed as is indicated by the one-dot, one-dash lines. This depletion layer 24' prevents the passage
50

of a reverse current.

The JBS rectifier shown in Fig. 2 is basically the same as that JBS rectifier shown in Fig. 1, in both structure and function, but different in that the P⁺-type silicon areas 18 are spaced from one another by such narrow gaps that they are connected together to reduce the reverse leak current when the reverse bias increases over a small value, for example a few volts.

The N⁻-type silicon layer 14 has an impurity concentration of, for example, 10^{16} atoms/cm³. The P⁺-type silicon areas 18 are arranged at the intervals of 6 μ m. Each P⁺-type silicon area 18 has a square upper surface contacting the metal film 22, each side being 5 μ m long, and has a depth of about 2 μ m. When a reverse bias V_R is 0 V, the depletion layers 24 has thickness of 0.35 μ m, and each portion of the N⁻-type silicon layer 14, which is interposed between the two adjacent P⁺-type silicon areas 18, has a width of 1 μ m.

The JBS rectifier shown in Fig. 2 is identical to the JBS rectifier shown in Fig. 1, except that more P⁺-type silicon areas 18 contact the barrier metal film 22. In either JBS rectifier, the layer of the Schottky junction defined by the barrier metal film 22 and those portions of the N⁻-type layer 14 which contact the film 22 is less than the total surface layer of the 14 by the sum of the layers of the P⁺-type areas 18. As has been pointed out, that portion of the N⁻-type silicon layer in which a P⁺-type silicon area is formed has a surface area of 36 μ m² ($= 6 \times 6 \mu$ m), and each P⁺-type silicon area has a surface area of 25 μ m² ($= 5 \times 5 \mu$ m). The surface area of each P⁺-type silicon area is 30.6% of the surface area of the upper surface of that portion of the N⁻-type silicon layer in which P⁺-type silicon area is formed. This means that the current efficiency of the substrate is not so high for the pellet size of the JBS rectifier.

One of the methods of increasing the current efficiency of the substrate is to reduce the surface areas of the P⁺-type silicon areas smaller. However, a reduction of the reverse breakdown voltage V_B must be prevented despite of the curvature of the PN junction, thereby to maintain the breakdown voltage V_B sufficiently high. To maintain a sufficient breakdown voltage V_B , a P⁺-type impurity must be diffused into the N⁻-type silicon layer to a relatively great depth. When the P⁺-type impurity is so diffused into the N⁻-type silicon layer, it is also diffused in horizontal direction, inevitably expanding the surface area of each P⁺-type silicon area. The surface area of each P⁺-type silicon area can hardly be reduced as much as is desired in order to increase the current efficiency of the substrate.

Fig. 3A represents the cross section which each depletion layer 24 has when a reverse bias of 0 V is applied to the JBS rectifier shown in Fig. 2, and Fig. 3B illustrates the distribution of electric charge ρ , the distribution of electric field E, and the distribution of potential ϕ which are observed in the JBS rectifier when a reverse bias of 0 V is applied to the JBS rectifier. Also, Fig. 4A shows the cross section which each depletion layer 24 has when a reverse bias of 3 V is applied to the JBS rectifier, and Fig. 4B illustrates the distribution of electric charge ρ , the distribution of electric field E, and the distribution of potential ϕ which are observed when a reverse bias of 3 V is applied to the JBS rectifier. In these figures, M designates the Schottky barrier metal film. Plotted on the x-axis in Fig. 3B and 4B is the depth of that portion of the substrate which is located between any two adjacent P⁺-type silicon areas 18.

As is evident from Figs. 3A and 3B, a specific charge is accumulated in the surface of the N⁻-type silicon layer 14 when a reverse bias V_R of 0 V is applied to the JBS rectifier. As is shown in Figs. 4A and 4B, the distribution of electric charge ρ has a square profile when a reverse bias voltage V_R of 3 V is applied to the JBS rectifier. In this case, the distribution of electric field E and the distribution of potential ϕ have similar profiles. The maximum intensity E_m of the electric field and the maximum potential V_d , both shown in Fig. 4B, are given:

$$E_m = -(qN_d W)/\epsilon_s$$

$$V_d = -(qN_d W^2)/(2\epsilon_s)$$

where N_d is the impurity concentration of the N⁻-type silicon layer, W is the width of the depletion layer, and ϵ_s is the dielectric constant of silicon.

As is understood from the profile of electric field (E) distribution has a high gradient. Therefore, the P⁺-type silicon layer cannot serve to provide adequate depletion-layer effect. The higher the breakdown voltage the JBS rectifier is to have, the deeper the P⁺-type silicon layer must be, and the lower the current efficiency the substrate inevitably has.

As has been described, the ordinary Schottky barrier diode, whose forward voltage is low and which can operate at high speed, have a low reverse breakdown voltage and a large reverse leakage current. The JBS rectifier, developed to have a high reverse breakdown voltage and a small reverse leakage current, has an N⁻-type silicon layer which defines a Schottky junction with the barrier metal film and whose surface area is smaller than the area of that portion of the N⁻-type silicon layer contacting the metal film by the sum of the areas of the P⁺-type silicon layers. The current efficiency of the substrate is inevitably low though that surface area of the substrate which contacts the barrier metal film is comparatively large. The

area at which each P⁺-type silicon layer contacts the barrier metal film may be reduced to increase the current efficiency, but can not be reduced so much since the reverse breakdown voltage of the JBS rectifier is directly proportional to said area.

The P⁺-type silicon layers can be arranged at longer intervals thereby to increase the area occupied by the N⁻-type silicon layer. However, the longer the intervals at which the P⁺-type silicon layers are arranged, the more the reverse leakage current.

It is the object of the present invention to provide a semiconductor device comprising a Schottky barrier diode, in which a PN junction is formed on a semiconductor layer located below a barrier metal film, the current efficiency of a substrate is high though that surface area of the substrate which contacts the barrier metal film is comparatively small, and the reverse voltage is not so high when a continuous depletion layer is formed, thereby decreasing a reverse leakage current.

According to the present invention, there is a semiconductor device: a semiconductor substrate having first and second major surfaces and including a first semiconductor layer of a first conductivity type, a second semiconductor layer of a first conductivity type formed on the first semiconductor layer and having an impurity concentration lower than that of the first semiconductor layer, and a third semiconductor layer formed between the first and the second, set in Schottky contact with the second metal film, and having an impurity concentration lower than that of the first semiconductor layer and lower than that of the second semiconductor layer; first metal film formed on the first major surface of the semiconductor substrate, and contacting the first semiconductor layer; second metal film formed on the second major surface of the semiconductor substrate; and a plurality of semiconductor areas of the second conductivity type, formed in the second major surface of the semiconductor substrate, contacting the second metal film, and extending through the second semiconductor layer and reaching at least the third semiconductor layer.

The aforementioned aspects and other features of the present invention are explained in the following description, taken in connection with the accompanying drawings, in which:

Fig. 1 is a sectional view showing a conventional semiconductor device;

Fig. 2 is a sectional view showing another conventional semiconductor device;

Figs. 3A and 3B are a schematic view showing the depletion layers formed in the conventional device shown in Fig. 2, and a diagram representing the relationship among the distribution of electric charge ρ , the distribution of electric field E, and the distribution of potential ϕ observed in the semiconductor device;

Figs. 4A and 4B are respectively a schematic view showing the depletion layer formed in the conventional device shown in Fig. 2 when the device is placed in a different condition (Figs. 3A and 3B), and a diagram representing the relationship among the distribution of electric charge ρ , the distribution of electric field E, and the distribution of potential ϕ observed in the device placed in the different condition;

Fig. 5 is a sectional view showing a semiconductor device according to the present invention;

Fig. 6 is a schematic representation of the substrate of the semiconductor device shown in Fig. 5;

Figs. 7A and 7B are a sectional view and a plan view, both illustrating the arrangement of the P⁺-type silicon areas of the device shown in Fig. 5;

Fig. 8 is a sectional view showing the depletion layers which are formed in the device illustrated in Fig. 5, when a reverse bias V_R of 0 V is applied to the device;

Fig. 9 is a sectional view showing a depletion layer which is formed in the device illustrated in Fig. 5, when a reverse bias V_R of a value greater than 0 V is applied to the semiconductor device;

Figs. 10A and 10B are a schematic view illustrating the depletion layers formed in the device shown in Fig. 5, and a diagram representing the relationship among the distribution of electric charge ρ , the distribution of electric field E, and the distribution of potential ϕ , which is observed in the device; and

Figs. 11A and 11B are respectively a schematic view showing the depletion layers formed in the device shown in Fig. 5 when the device is placed in a different condition (Figs. 10A and 10B), and a diagram representing the relationship among the distribution of electric charge ρ , the distribution of electric field E, and the distribution of potential ϕ observed in the device placed in the different condition.

Some preferred embodiments of the invention will now be described with reference to the accompanying drawings.

Fig. 5 is a cross-sectional view illustrating a junction barrier-controlled Schottky (JBS) rectifier according to one embodiment of the present invention. The JBS rectifier has a semiconductor layer, cathode electrode film 32 formed on the lower surface of the semiconductor substrate 30, and an anode electrode film 34 formed on the upper surface of a semiconductor substrate 30. The lower surface of the cathode electrode film 32 defines one major surface of the substrate 30, whereas the anode electrode film 34 defines the other major surface of the substrate 30.

As shown in Fig. 6, the semiconductor layer is comprised of a semiconductor layer 36 (hereinafter called "N⁻-type layer") of a first conductivity type (i.e., N-type) formed on the cathode electrode film 32, a

semiconductor layer 38 (hereinafter called "N⁻-type layer") of the first conductivity type formed on the N⁺-type layer 36 and having an impurity concentration (i.e., 10^{16} atoms/cm³), a semiconductor layer 40 of the first conductivity type (hereinafter called "N⁻⁻⁻-type layer") formed on the N⁻-type layer 38 and having an impurity concentration (i.e., 10^{14} atoms/cm³) lower than that of the N⁻-type layer 38, and a semiconductor layer 42 of the first conductivity type (hereinafter called "N⁻-type layer") formed on the N⁻⁻⁻-type layer 40 and having an impurity concentration (i.e., 10^{16} atoms/cm³). The four silicon layers, i.e., the N⁻-type layer 36, the N⁻-type layer 38, the N⁻⁻⁻-type layer 40, and the N⁻-type layer 42 are made of single-crystal silicon.

The anode electrode film 34 is made of a Schottky-barrier metal such as titanium (Ti, Mo, V), and is formed in the opening of an oxide film 44 which is formed on the second major surface of the substrate 30. A plurality of semiconductor areas 46 that of the substrate 30 is formed in the second major surface of the substrate. These areas 46 (hereinafter referred to as "P⁺-type layers") has the conductivity type opposite to that of the substrate 30. They contact the anode electrode film 34 and extend downward through the N⁻-type layer 42 and the N⁻⁻⁻-type layer 40 and into the N⁻-type layer 38. A guard ring layer 48 (hereinafter called "P⁺-type layer") is formed in the surface of the substrate 30, surrounding that portion of the substrate 30 in which the P⁺-type areas 46 are formed. The P⁺-type layer 48 increases the withstand voltage of the JBS rectifier. A channel stopper layer 50 (hereinafter referred to as "N⁺-type layer") is also formed in the surface of the substrate 30, surrounding the P⁺-type layer 48, thereby preventing a depletion layer from expanding in the horizontal direction in the substrate 30. If necessary, a P⁺-type layer, or a high-voltage termination layer, can be formed in the surface of the substrate 30 and between the P⁺-type layer 48 and the N⁺-type layer 50.

The JBS rectifier shown in Figs. 5 and 6 is manufactured by means of the known method. As is illustrated in Fig. 6, the N⁻-type layer 38 having a thickness of 3 to 4 μ m is formed on the N⁻-type layer 36 (i.e., a semiconductor wafer). Then, the N⁻⁻⁻-type layer 40 having a thickness of 1 μ m is formed on the N⁻-type layer 38. Next, the N⁻-type layer 42 having a thickness of 1 μ m is formed on the N⁻⁻⁻-type layer 40. The layers 38, 40, and 42 are formed by means of epitaxial growth such that they have the impurity concentrations specified above. Alternatively, the layer 42 can be formed by implanting ions of the impurity into the surface of the layer 40. In this case, the layer 40 must be 2 μ m thick.

Thereafter, the oxide film 44 is formed on the N⁻-type layer 42. Phosphorus (P) are implanted into the substrate 30 by a known method, thereby forming the N⁻-type layer 50. Further, boron (B) are implanted into the substrate 30, thus forming the P⁺-type areas 46 and the P⁺-type layer 48. Titanium (Ti, Mo, V) is deposited in the opening of the oxide film 44 by means of sputtering or vapor deposition, and aluminum (Al) is deposited, thereby forming the anode electrode film 34.

As can be understood from the above, the JBS rectifier has a substrate 30 consisting of four semiconductor layers, i.e., the N⁻-type layer 36, the N⁻-type layer 38, the N⁻⁻⁻-type layer 40, and the N⁻-type layer 42. It further comprises a plurality of P⁺-type areas 46 formed in the second major surface of the substrate 30, the areas 46 extending downward through the N⁻-type layer 42 and the N⁻⁻⁻-type layer 40 into the N⁻-type layer 38.

In operation, a forward bias is applied between the anode electrode film 34 and the cathode electrode film 32, generally at the value of voltage as the current begin to flow that of SBD is smaller than that of PN junction diode. Then, a current flows from the film 34 through the N⁻-type layer 42, the N⁻⁻⁻-type layer 40, the N⁻-type layer 38, and the N⁺-type layer 36. The current finally flows into the cathode electrode film 32. As a result, the forward-voltage drop decreases, and the JBS rectifier exhibits a forward-voltage characteristic very similar to that of the ordinary Schottky-barrier diode.

In Fig. 5, the two-dots, one-dash lines indicate the regions 52 through which currents should flow if no depletion layers were formed in the substrate 30. Actually, a depletion layer is formed in the PN junction of the JBS rectifier. Table 1, which is an excerpt from a publication (i.e., a "Si data" book), shows the relationship which the impurity concentration of an N-type layer and the width of a depletion layer formed in the N-type layer have when the N-type layer forms a step-shaped PN-junction jointly with the high impurity of P-type region. The N-type layer is equivalent to the N⁻⁻⁻-type layers 38 and 42 and also to the N⁻⁻⁻-type layer 40. The N⁻⁻⁻-type layers 38 and 42 have an impurity concentration of 10^{16} atoms/cm³, whereas the N⁻⁻⁻-type layer 40 has an impurity concentration of 10^{14} atoms/cm³. A reverse bias V_R applied to the N⁻-type layers 38 and 42, and the N-type layer is 0 V, or 40 V whereas a reverse bias V_R applied to the N⁻⁻⁻-type layer 40 is 10 V.

Table 1

Impurity Concentrations of N-type Layers (atoms/cm ³)	Widths of Depletion Layers (μm)	
	V _R = 0 V	V _R = 10 V
10 ¹⁶	0.35	1
10 ¹⁴	3.5	10
Note: V _R is the reverse bias.		

As is evident from Table 1, the depletion layer formed in the N⁻-type layer 40 is about ten times wider than the depletion layer formed in the N⁻-type layers 38 and 42. The locations of the P⁺-type areas 46 are determined in accordance with the data shown in Table 1 to satisfy two specific conditions. The first condition is that a depletion layer formed in the N⁻-type layer 40 when a low reverse bias (including 0 V) is applied to the JBS rectifier pinches off the current path and that does not pinch off the current path when a forward bias is applied. The second condition is that the area in which the anode electrode film 34 contacts the N⁻-type layer 42, thus defining a Schottky contact, is as much greater than the contact area between the P⁺-type area 46 and the substrate 30 as is possible.

Further, the P⁺-type area 46 is formed such that the depletion layers formed in the substrate 30 when a forward bias is applied are not connected one another to pinch off the path of the forward current, and also that the depletion layers formed in the substrate 30 when a reverse bias is applied are connected one another to pinch off the path of the reverse leakage current.

Figs. 7A and 7B are views illustrating the arrangement of the P⁺-type areas 46. As is shown in these figures, the upper surface of each P⁺-type area 46 is a square whose sides have a length l_1 . The areas 46 are spaced apart from one another for a distance of l_2 . In this embodiment, l_1 and l_2 are, for example, 5 μm and 10 μm, respectively. The areas 46 have a depth of about 2 μm. When a reverse bias V_R of 0 V is applied to the JBS rectifier, a depletion layer having a thickness of 3.5 μm will be formed around each P⁺-type area 46. In this case, that portion of the N⁻-type layer 42 which is located between any two adjacent P⁺-type areas 46 will have a width of 5 μm.

The region allotted to each area 46 has an area of 100 μm² (= 10 μm × 10 μm). Of this area, 25 μm² is occupied by the area 46. Hence, the area in which the N⁻-type layer 42 contacts the anode electrode film 34 is 75% of the area of the region allotted to each area 46. This value of 75% is much greater than in the conventional JBS rectifier, and the substrate 30 has a current efficiency much higher than that of the substrate of the conventional JBS rectifier.

When the reverse bias is applied between the anode electrode film 34 and the cathode electrode film 32, the PN junction located between each P⁺-type area 46 and the N⁻-type layer 40 is reverse-biased, and a depletion layer develops and expands into the N⁻-type layer 40 which has a low impurity concentration. Finally, the depletion layers formed in the layer 40 contact one another, forming a single depletion layer. This depletion layer pinches off the current path, thereby decreasing the increase of the reverse leakage current. Therefore, the JBS rectifier has a reverse-current characteristic which is extremely similar to that of the ordinary junction diode.

The reverse bias for pinching off the current path should be as low as possible, in order to improve the reverse-current characteristic of the JBS rectifier. As has been pointed out, the N⁻-type layer 40 has a low impurity concentration, so that the current path is pinched off when a low reverse bias including 0 V is applied between the anode electrode film 34 and the cathode electrode film 32. On the other hand, the N⁻-type layers 42 have an impurity concentration higher than that of the N⁻-type layer 40, so that a desired Schottky barrier is formed to allow only a relatively small forward voltage drop. In other words, the N⁻-type layer 40 having a low impurity concentration serves to pinch off the current path, whereas the N⁻-type layers 42 serve to form a desired Schottky barrier. Any two adjacent P⁺-type areas 46 can be and actually so wide a gap in the N-layer as the current path need not be pinched off when the reverse bias is applied to the JBS rectifier. Since the gap between any two adjacent P⁺-type areas 46 is wide, that surface area of each N⁻-type layer 42 which forms a Schottky junction is sufficiently large.

Fig. 8 is a diagram showing the depletion layers 56 which are formed when a reverse bias V_R of 0 V is applied to the JBS rectifier (Fig. 5). Fig. 9 is a diagram illustrating the depletion layer 56 which is formed

when a reverse bias V_R higher than 0 V is applied to the JBS rectifier (Fig. 5).

In the case shown in Fig. 8, that portion 58 of the layer 40, which is located between the two depletion layers 56 formed around any adjacent P^+ -type areas 46, serves as a current path. This current path (i.e., the portion 58) expands when a forward bias is applied to the JBS rectifier, and a forward current is thereby made to flow. Therefore, the substrate therefore has a high current efficiency, and the JBS rectifier exhibits a forward-current characteristic extremely similar to that of the conventional SBD rectifier. If the current path (i.e., the portion 58) is formed when forward bias is applied to the JBS rectifier. The depletion layers 56 can expand through out the N^- -type layer 40, thus forming a single depletion layer. Even in this case, current paths are secured since the N^- -type layer 42 has some portions in which no depletion layers are formed.

In the case shown in Fig. 9, a single depletion layer 56 is formed in the layers 38, 40, and 42 since the reverse bias V_R is higher than 0 V. The depletion layer pinches off the current paths. As a result, the increase of the reverse leakage current decreases which has resulted from the Schottky junction. The reverse-current characteristic of the JBS rectifier is improved, becoming very similar to the reverse leakage-current characteristic of the ordinary PN-junction diode.

In the embodiment shown in Fig. 5, the P^+ -type areas 46 can be formed in the layers 42 and 40 only, not extending into the N^- -type layer 38. Also, the P^+ -type areas 46 can take a shape different from that shown in Figs. 7A and 7B. Furthermore, the substrate 30, which consists of four layers 36, 38, 40 and 42, can be replaced by one which consists of three layers, e.g., an N^+ -type layer, an N^- -type layer formed on the N^+ -type layer, and an N^- -type layer formed on the N^- -type layer. If this is the case, the areas 46 can be formed through the N^- -type layer and in the N^- -type layer, whereby the same advantage is ensured as by the substrate 30 comprised of the four layers 36, 38, 40, and 42.

Generally, the lower the impurity concentration of a semiconductor layer contacting a Schottky-barrier metal film, the higher the Schottky barrier is formed in the semiconductor layer. Hence, a Schottky barrier formed in an N^- -type layer contacting a barrier metal film is higher than a Schottky barrier formed in an N^+ -type layer, and causes a greater forward voltage drop. Hence, when the substrate 30 is comprised of an N^+ -type layer, an N^- -type layer on the N^+ -type layer, and an N^- -type layer on the N^- -type layer, the depletion layer is thin, and the electric field within the depletion layer has a high gradient. Consequently, the depletion layer cannot withstand a high reverse voltage. In other words, the barrier effect of the depletion layer decreases. Nonetheless, this problem does not arise if the three-layer substrate is of N^- -type, beside anode metal N^- , N^- , N^- -types. Needless to say, the problem does not arise in the JBS rectifier shown in Fig. 5, wherein the N^- -type layer 42 contact the anode electrode film 34.

Figs. 10A and 10B are a schematic view showing the depletion layers formed in the JBS rectifier when a reverse voltage of 0 V is applied to the rectifier, and a diagram representing the relationship which the distribution of electric charge ρ , the distribution of electric field E and the distribution of potential ϕ have when a reverse bias of 0 V is applied to the JBS rectifier. On the other hand, Figs. 11A and 11b are a schematic view showing the depletion layers formed in the JBS rectifier when a reverse bias of 3 V is applied to the JBS rectifier, and a diagram representing the relationship which the distribution of electric charge ρ , the distribution of electric field E and the distribution of potential ϕ have when a reverse bias of 3 V is applied to the JBS rectifier. In Figs. 10A, 10B, 11A and 11b, M designates the Schottky-barrier metal film. In Figs. 10A and 11A, the thickness of that portion of the substrate 30 which is located between any two adjacent P^+ -type areas 46 is plotted on the x axis.

As is evident from Figs. 10A and 10B, a specific amount of electrical charge is accumulated in the surface of the N^- -type layer 42 when a reverse bias of 0 V is applied to the JBS rectifier. In contrast, as is evident from Figs. 11A and 11b, an electrical charge is dispersed through the N^- -type layer 42 into the N^- -type layer 40 when a reverse bias of 3 V is applied to the JBS rectifier. Thus, the profile of charge-distribution extends horizontally, whereby the distributions of electric field and potential have gradients more gentle than those in the conventional device (Fig. 4B). The depletion layers formed around the P^+ -type areas can serve to improve the reverse-current characteristic of the JBS rectifier.

As has been described, in the JBS rectifier according to the present invention, a desired Schottky barrier is formed in the N^- -type layer contacting the Schottky-barrier metal film, and the N^- -type layer serves to pinch off the current path when a reverse bias is applied to the JBS rectifier. Therefore, the area occupied by those portions of the N^- -type layer which contact the Schottky-barrier metal film increases, and the JBS rectifier has a high current efficiency for its pellet size and an improved reverse-current characteristic.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor device comprising: a semiconductor substrate having first and second major surfaces and including a first semiconductor layer of a first conductivity type, and a second semiconductor layer of the first conductivity type having an impurity concentration lower than that of the first semiconductor layer, first metal film formed on the first major surface of said semiconductor substrate, and contacting said first semiconductor layer, second metal film formed on the second major surface of said semiconductor substrate; and a plurality of semiconductor areas of the second conductivity type, formed in the second major surface of said semiconductor substrate, contacting said second metal film, said semiconductor areas of the second conductivity type being formed in said second semiconductor layer and reaching at least said second semiconductor layer, characterized in that a third semiconductor layer (40) is interposed between said first semiconductor layer (36) and said second semiconductor layer (42) and having an impurity concentration lower than that of said first semiconductor layer (36), and said semiconductor areas (46) of the second conductivity type extend through said second semiconductor layer (42) into at least said third semiconductor layer (40).
2. A device according to claim 1, characterized in that said semiconductor areas (46) of the second conductivity type are located such that discrete depletion layers (56) are formed around the respective semiconductor areas (46) of the second conductivity type when a forward bias is applied to said semiconductor substrate (30), and a continuous depletion layer (56) contacting the semiconductor layers of the second conductivity is formed when a reverse bias is applied to said semiconductor substrate (30).
3. A device according to claim 1, characterized by further comprising a fourth semiconductor layer (38) of the first conductivity type interposed between said first and third semiconductor layers (36, 40) and having an impurity concentration lower than that of said first semiconductor layer (36) and higher than that of said third semiconductor layer (40).
4. A device according to claim 3, characterized in that the impurity concentrations of said second and fourth semiconductor layers (42, 38) are at most 10^{16} atoms/cm³, and the impurity concentration of said third semiconductor layer (40) is at most 10^{14} atoms/cm³.
5. A device according to claim 3, characterized in that said second and third semiconductor layers (42, 40) have a thickness of about 1 μ m, and said fourth semiconductor layer (38) has a thickness of about 3 to 4 μ m.
6. A device according to claim 1, characterized in that any two adjacent ones of said semiconductor areas (46) of the second conductivity type are spaced apart from each other for a distance equal to the width of the adjacent semiconductor areas (46).
7. A device according to claim 1, characterized in that said first semiconductor layer (36) is made of N⁺-type silicon, said second semiconductor layer (42) is made of N⁻-type silicon, said third semiconductor layer (40) is made of N⁻-type silicon, and said semiconductor areas (46) of the second conductivity type are made of P⁺-type silicon.

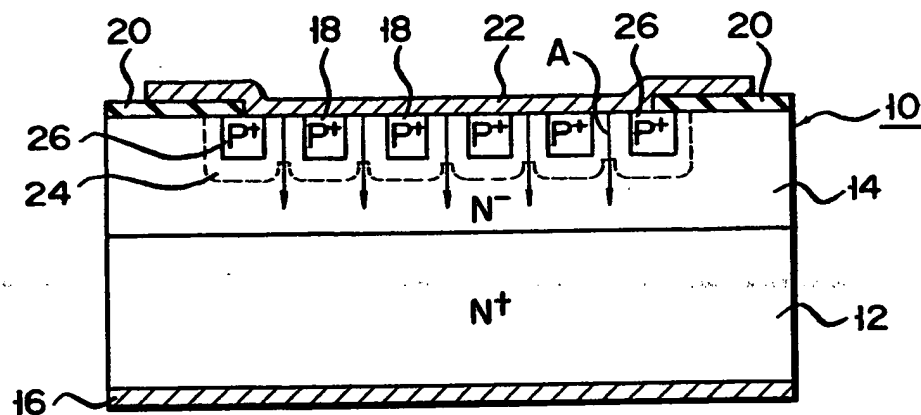
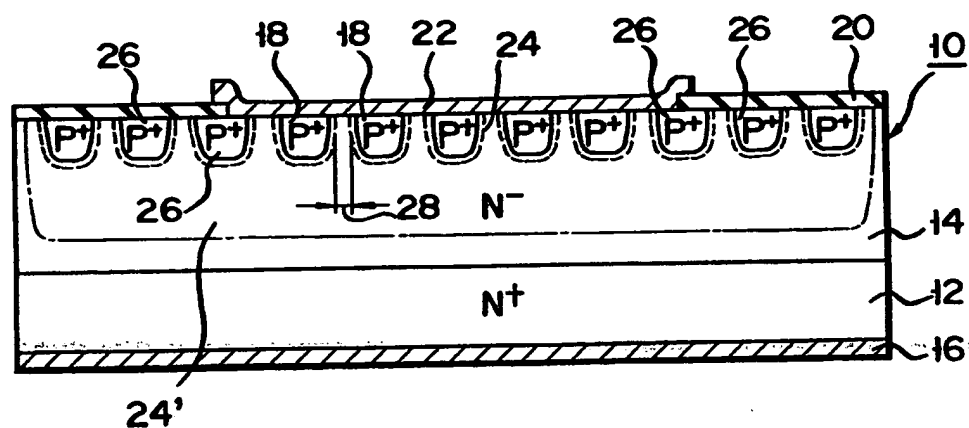


FIG. 1



F I G. 2

FIG. 3A

$V_R = 0[V]$

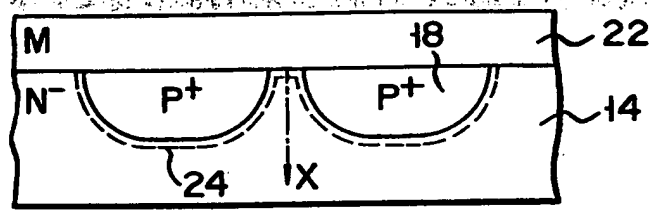


FIG. 3B

$V_R = 0[V]$

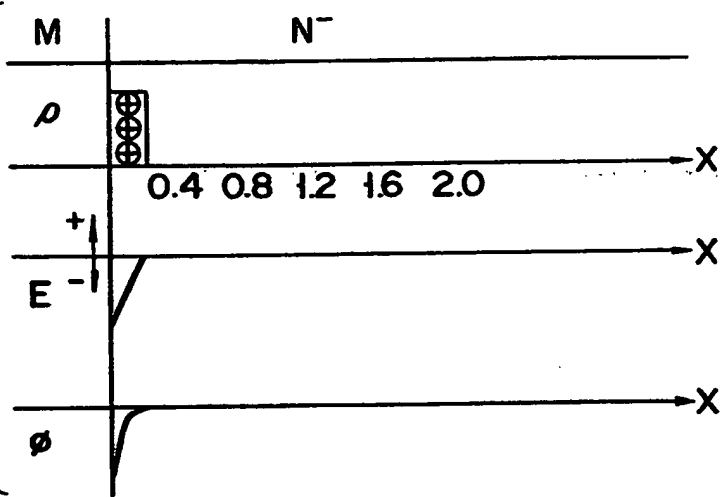


FIG. 4A

$V_R = 3[V]$

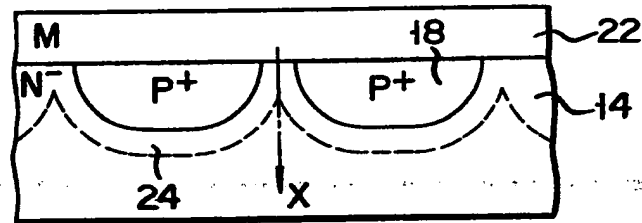
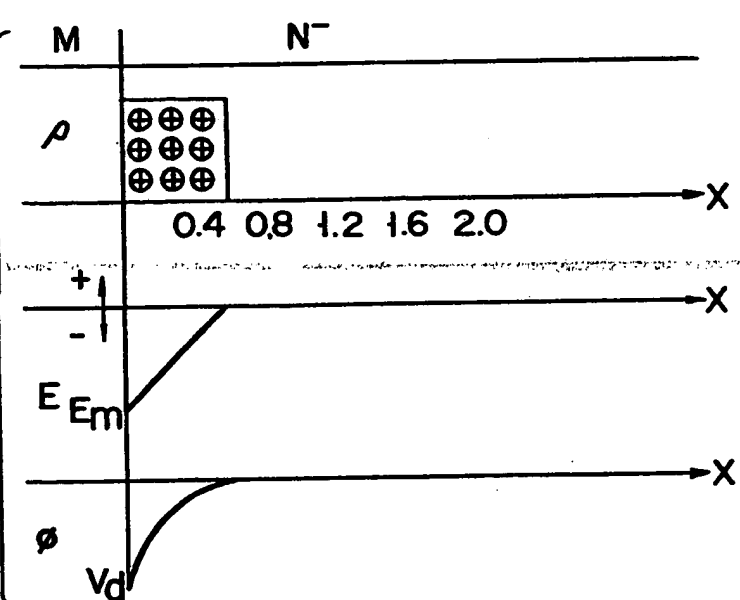


FIG. 4B

$V_R = 3[V]$



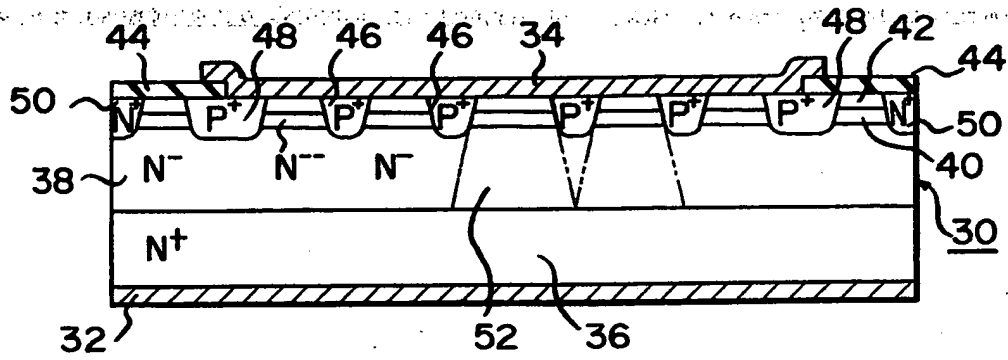


FIG. 5

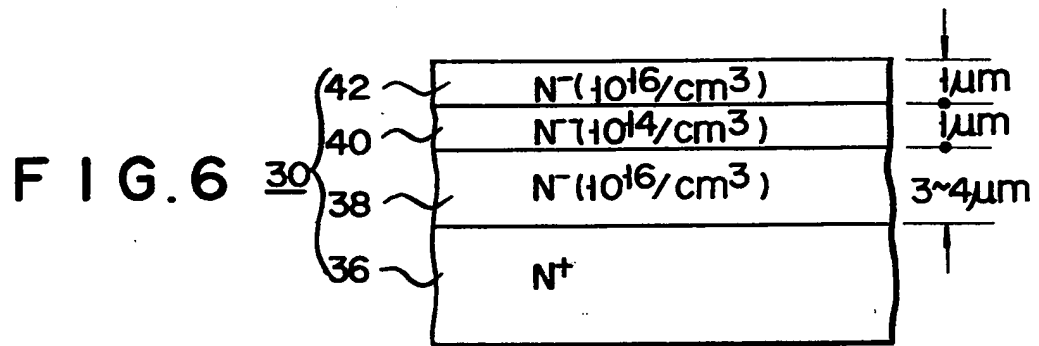


FIG. 7A

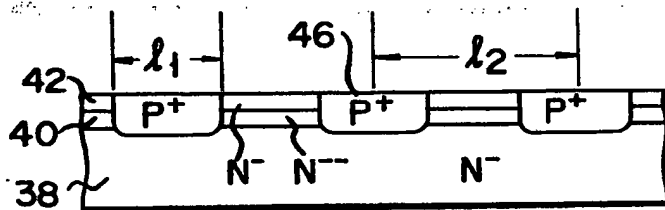
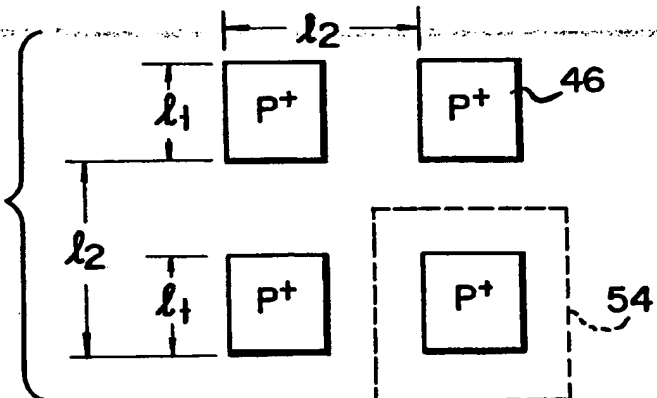


FIG. 7B



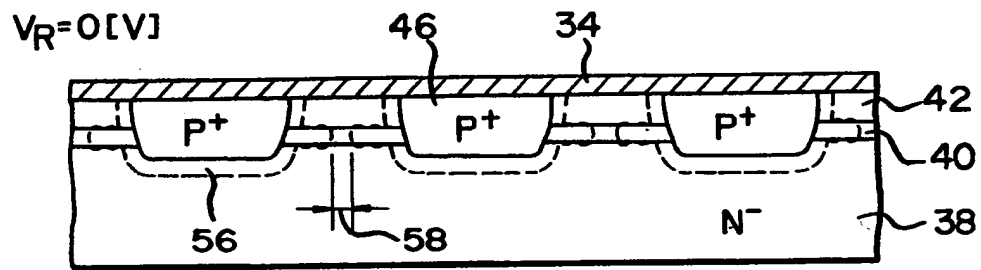


FIG. 8

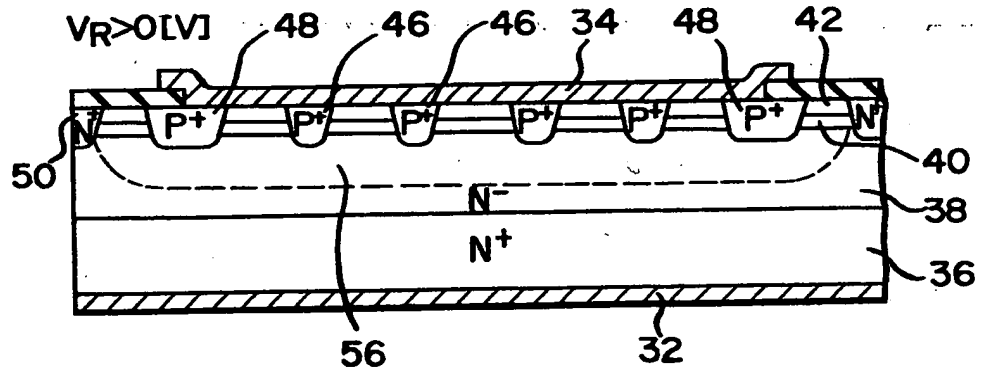


FIG. 9

FIG. 10A

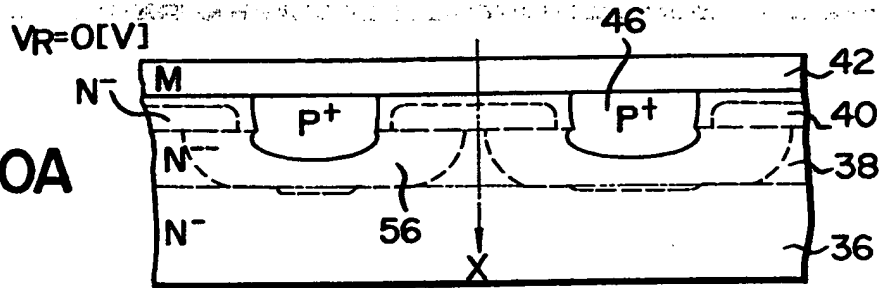


FIG. 10B

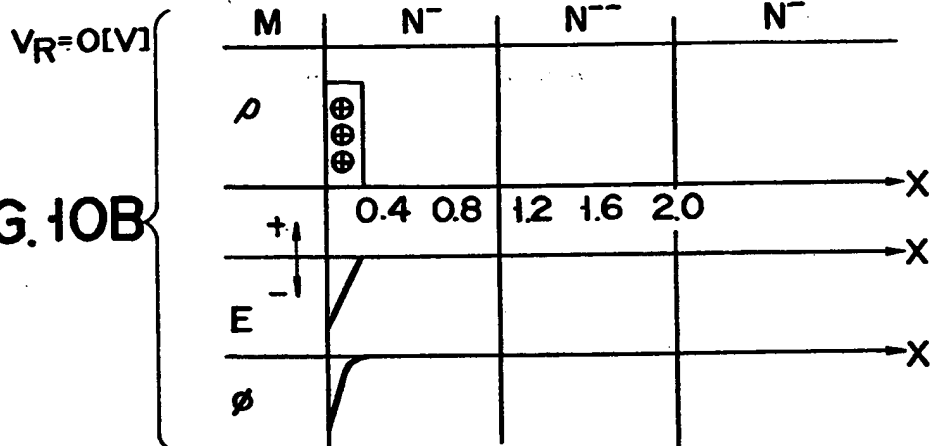


FIG. 11A

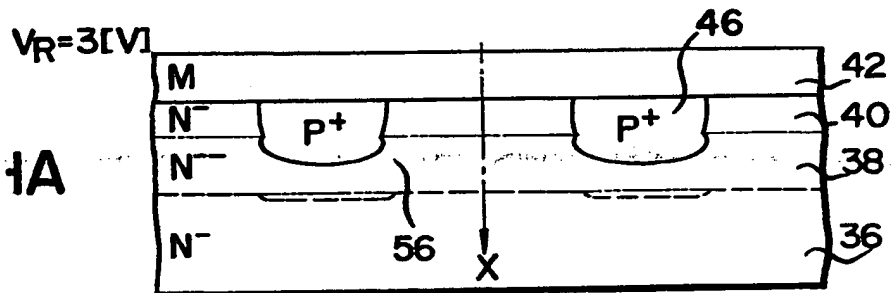
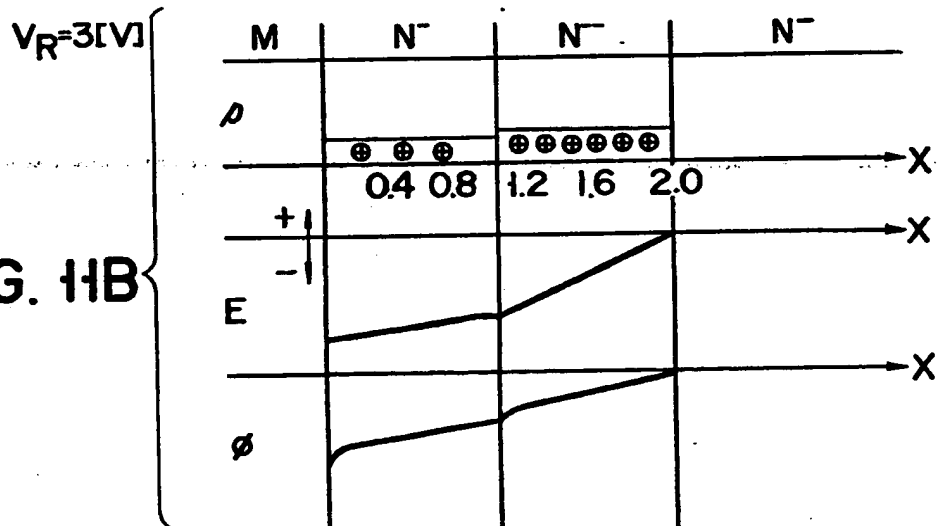


FIG. 11B





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Office

EUROPEAN SEARCH REPORT

Application number

DOCUMENTS CONSIDERED TO BE RELEVANT			EP 89122233.3
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.)
A	<u>US - A - 4 641 174</u> (BALIGA) * Fig. 1,3,4,5; column 3, line 19 - column 4, line 55 * D,A & JP-A2-60-74 582 ---	1,2,6, 7	H 01 L 29/91 H 01 L 29/48
A	<u>EP - A1 - 0 147 893</u> (PHILIPS) * Fig. 2; page 5, lines 17-37 * ---	1,2,3, 7	
A	<u>GB - A - 2 176 339</u> (PHILIPS) * Fig. 1,3,4; abstract * ---	1,2,6, 7	
A	<u>US - A - 4 134 123</u> (SHANWOW) * Fig. 1,5,8; claims * ---	1,2,3, 6,7	
A	<u>US - H - 40</u> (BUCHANAN) * Fig. 2; column 3, line 54 - column 4, line 49 * ---	1,7	TECHNICAL FIELDS SEARCHED (Int. Cl.) H 01 L
A	PATENT ABSTRACTS OF JAPAN, unexamined applications, E section, vol. 5, no. 91, June 13, 1981 THE PATENT OFFICE JAPANESE GOVERNMENT page 17 E 61 * Kokai-no. 56-35 473 * ---	1,6,7	
A	<u>US - A - 3 982 264</u> (ISHITANI) * Fig. 3,7; abstract * ---	1,3,6, 7	
A	<u>EP - A2/A3 - 0 103 138</u> (HITACHI)	1,3,7	
The present search report has been drawn up for all claims			
Place of search VIENNA		Date of completion of the search 20-02-1990	Examiner HEINICH
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

**Application number**

EP 89122233.3

DOCUMENTS CONSIDERED TO BE RELEVANT			EP 89122233.3
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.)
	<p>* Fig. 1,10,12; page 18, line 21 - page 19, line 25 *</p> <p>-----</p>		
			TECHNICAL FIELDS SEARCHED (Int. Cl.)
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
VIENNA	20-02-1990	HEINICH	
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